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| EXAMINER | |
|---|---|
| DILLON, SAMUEL A | |

| ART UNIT | PAPER NUMBER |
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| 2185 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/653,754 | MEIER ET AL. | |
| | Examiner | Art Unit | |
| | SAMUEL DILLON | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-13 and 15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13 and 15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's submission filed on July 15, 2009 has been entered. Per the amendment, Claims 1, 3, 11-13, 23-27 and 29 have been amended. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

## I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

2. Applicant's arguments with respect to the 35 U.S.C. 102(b) and 103(a) rejections of Claims 1, 3-11 and 23-29 have been fully considered and are **persuasive**. However, the rejections are moot under the interpretation given the reference as applied to the claim below. The Examiner notes that a slightly different interpretation and mapping of Tran has been used in the following rejections. Additionally, further review and interpretation of Claims 13 and 15-22 and the prior art of record has warranted their rejection below. The Examiner respectfully apologizes for any undue inconvenience.

3. **The Applicant contends *(pg 10, response filed 3/9/2009)* that Tran does not disclose predicting a first way to be hit in the cache for the first address responsive to the first value matching one of a plurality of values, wherein the one of the plurality of values is output from the first way of the memory.** The Examiner respectfully disagrees. Tran discloses predicting a first way *(it predicts it to be a hit, "way prediction", figure 5)* to be hit in the cache for the first address responsive to the first value *(Decode[0], figure 5)* matching one of a plurality of values *(each value comprises either the first, second, etc, of the Row Drive's of each given Decode[i], figure 5, Decode[0] matches the first value when one of the first 4 rows is picked for a given way prediction)*, wherein the one of the plurality of values is output from the first way of the memory *(figure 5)*.

4. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

## II. REJECTIONS BASED ON PRIOR ART

### ***Claim Rejections - 35 USC ' 102 - Tran***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1, 3-11, 13, 15-21 and 23-29** are rejected under 35 U.S.C. 102(b) as being anticipated by Tran *(US Patent No. 6,016,533)*.

7. As per **Claims 1 and 13**, but more specifically to Claim 1, Tran discloses a way predictor comprising:

a decoder *(set of multiplexers 78A-78D, figure 5)* that decodes an indication of a first address *(Index[1:0], figure 5)* that is to access a cache for a current cache access during use, the decoder selecting a set responsive to the indication of the first address during use *(selects one of Rows 0-3, figure 5)*;

a memory *(set of way prediction memory locations, each location stores 1 bit, "Row X, Way Y", figure 5)* coupled to the decoder, wherein the memory outputs a

plurality of values *(each value is the set of all of the given way predictions outputted from the multiplexers, so value '0' would be the bits output from multiplexor 78A, 78E, etc figure 5)* from a set of storage locations *(either first row, second row, etc, figure 5)* in response to the decoder selecting the set during use, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory *(each multiplexer outputs from a block associated with a single way, so the set of four outputs a set of values that are each associated with a different way, elements 78A-78D, figure 5)*, wherein the cache includes a same number of ways as the memory *(each include 4 total ways, figure 5)* , and wherein the cache includes a tag memory *(element 70, figure 4)* storing a plurality of tags corresponding to cache lines stored in the cache and a data memory *(element 50, figure 4)* storing the cache lines during use, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache in a respective way of the plurality of ways and in the set *(interpreted as meaning that the plurality of bits are in the set, the values associated with rows 0-3 are 1 bit, but there are a plurality of sets of 4 rows outputted, figure 5)*; and

a circuit *(set of Row Drive's, figure 5)* coupled to receive the plurality of values and a first value *(Decode[0], figure 5)* corresponding to the first address, wherein the circuit compares the first value to the plurality of values during use *(each of Row Drive(n) is an AND operation, figure 5)*, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way be a hit in the cache for the first address for the current access during use *(if both values are true, it selects that way as the output for a given row, figure 5)*, and wherein the circuit outputs a way identifier *(the way identifier is the 4 bit output of the set of decoders for a given row, which actives the specific way of a given row, figure 5)*

identifying the first way to the data memory during use, the way identifier used by the data memory to select the first way to output data during use *(the output of Row Drive(n)'s select the ways of the cache, figure 5)*, and wherein the circuit constructs the way identifier based on the comparisons of the first value to the plurality of values during use *(it constructs the identifier based on the comparisons of the outputted way predictions for a given row, figure 5)*.

8. For **Claims 3 and 15**, but more specifically to Claim 3, Tran discloses the circuit, if none of the plurality of values matches the first value, asserts an early miss signal during use *(in the case that decoder 62 does not select that row, figure 5)*.

9. For **Claim 4 and 16**, but more specifically to Claim 4, Tran discloses each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag *(column 3 lines 22-24, column 13 lines 10-20; a cache line is read and output by the sense amp unit, if the requested address hits in the tag cache, the way prediction is verified by the comparator which receives the way prediction after it is selected from the way prediction array, column 14 lines 34-39; offset bits from a request address are used to select the requested bytes from the cache line, column 14 lines 35-36)*.

10. For **Claim 5 and 17**, but more specifically to Claim 5, Tran discloses each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line *(the output of the multiplexers is derived from Index[1:0], figure 5)*.

11. For **Claim 6 and 18**, but more specifically to Claim 6, Tran discloses each of the plurality of values comprises a portion of one or more address operands used to generate the address *(the output of the multiplexers is derived from Index[1:0], figure 5)*.

12. For **Claim 7 and 19**, but more specifically to Claim 7, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of the address *(inherent*

*in that the multiplexers are implemented in logical circuits, to select one of them would involve performing a logical combination of two or more logical values, two of which are Index[1:0], figure 5)*.

13. For **Claim 8 and 20**, but more specifically to Claim 8, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address *(one of the outputs is a 1, the rest are 0's, so no matter what combination Index[1:0]'s bits are, one of the outputs is a logical combination of both of them, figure 5)*.

14. For **Claim 9 and 21**, but more specifically to Claim 9, Tran discloses the indication of the first address comprises at least a portion of the first address *(Index[1:0], figure 5)*.

15. For **Claim 10**, Tran discloses the indication of the first address comprises two or more address operands used to generate the first address *(Index[1:0] is 2 bits, figure 5)*.

16. For **Claim 11**, Tran discloses if the way prediction is incorrect, the cache replaces a cache line in the way indicated by the way prediction with a missing cache line corresponding to the first address during use *(if there is no match found in the tags, a miss occurs, and the output data is canceled and the requested data is fetched from main memory, col. 15 lines 31-33)*.

17. For **Claim 23**, Tran discloses an apparatus comprising the way predictor of Claim 1, and the data cache data memory *(element 50, figure 4)* coupled to the way predictor, wherein the data cache data memory is arranged into the plurality of ways *(see element 50, figure 4)*, and wherein the data cache data memory outputs data from the first way during use, and wherein the data cache data memory includes a second circuit that reduces power consumption attributable to one or more non-predicted ways of the plurality of ways during use *(die space and power consumption may be reduced through the use of one sense amp unit instead of multiple sense amp units, i.e. one sense amp unit per way or column, col. 3 lines 8-16)*.

18. For **Claim 24**, Tran discloses the data cache tag memory outputting a tag from the first way and not outputting tags from the one or more non-predicted ways during use *(in the case that the way is validated, figure 4)*.

19. For **Claim 25**, Tran discloses the second circuit generates separate wordlines for each of the plurality of ways in the data cache data memory during use, and wherein the second circuit activates a first wordline to the first way and to not activate word lines to the non-predicted ways during use *(the Row Drive(n)'s pick word lines based on the predicted way from the set of word lines that could be outputted, figure 5)*.

20. For **Claim 26**, Tran discloses the second circuit includes column multiplexor circuitry *(column select 82 and element 84 and the like, figure 5)* coupled to the plurality of ways, wherein the column multiplexor circuitry selects the output of the first way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the predicted first way *(one of the inputs is a result of the predicted first way, so can be said to be controller by said way, figures 4 and 5)*.

21. For **Claim 27**, Tran discloses the second circuit includes column multiplexor circuitry *(column select 82 and element 84 and the like, figure 5)* coupled to the plurality of ways, wherein the column multiplexor circuitry selects the output of the first way as input to a sense amplifier circuit during use, wherein the column multiplexor circuitry is controlled by the predicted first way *(one of the inputs is a result of the predicted first way, so can be said to be controller by said way, figures 4 and 5)*.

22. For **Claim 28**, Tran discloses the second circuit comprises a plurality of sense amplifier circuits *(col. 14 lines 5-16)*, wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the predicted first way *(figures 4 and 5)*.

23. For **Claim 29**, Tran discloses the apparatus further comprising a second level cache *(the Examiner takes official notice that cache hierarchies are well known in the art, and that it would have been obvious to include a second level cache for the benefit of additional caching)*, and wherein the circuit detects a miss responsive to the plurality of values and the first value prior to the miss being detected in the cache that corresponds to the data cache data memory during use *(a miss that happened prior to the current access, possibly unrelated, column 1 lines 40-57)*, and wherein the circuit signals the miss to the second level cache during use, and wherein the second level cache begins an access corresponding to the first address responsive to signal from the circuit during use *(reading a value from a cache, column 1 lines 40-57)*.

## ***Claim Rejections - 35 USC ' 103 – Tran and Wickeraad***

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. **Claim 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran *(US Patent No. 6,016,533)* in view of Wickeraad et al *(US Patent No. 6,4901654)*.

26. For **Claims 12 and 22**, but more specifically to Claim 12, Tran fails to disclose if no way prediction is generated and a cache miss results for the first address, the cache uses a replacement algorithm to select the cache line to be replaced with the missing cache line during use. Wickeraad discloses a cache memory replacement algorithm that replaces cache lines based on the likelihood that cache lines will not be needed soon *(col. 4, lines 50- 52)*.

Tran and Wickeraad are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Wickeraad suggests that it would have been

desirable to incorporate a cache line replacement algorithm into the system of Tran because this allows data which is likely needed soon is assigned a higher replacement class, while data that is more speculative and less likely to be needed soon is assigned a lower replacement class *(col. 5, lines 2-6)*. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Tran as suggested by Wickeraad to incorporate the feature as claimed.

## III. CLOSING COMMENTS

### a. STATUS OF CLAIMS IN THE APPLICATION

27. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

#### a(1). CLAIMS NO LONGER IN THE APPLICATION

28. Claims 2 and 14 were cancelled by amendment.

#### a(2). CLAIMS REJECTED IN THE APPLICATION

29. Claims 1, 3-13 and 15-29 have received a non-final action on the merits.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application is assigned is 571-273-8300.

***IMPORTANT NOTE***

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hong Kim/
Primary Examiner, Art Unit 2185

Sam Dillon
Examiner
Art Unit 2185